Abstract of the Disclosure

A circuit and method for programming phase-change memory devices, such as chalcogenide memory (PRAM), are described. The invention is directed to an approach to programming PRAM elements from a reset state to a set state or from a set state to the set state. The invention provides a novel and nonobvious PRAM device and method in which a set pulse duration time is controlled by monitoring the state of the memory element during programming such as by comparing the voltage of a bit line with a reference voltage or comparing the cell resistance with a set state cell resistance. The duration of the set pulse is controlled in response to the detected state of the memory element. The result of the approach of the invention is the significant reduction in PRAM programming errors, such as those caused by a constant-duration set pulse, as well as reduction in programming time duration and power consumption.

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